In the Claims:

Please amend claims as indicated below. This listing of claims replaces all prior versions.

1. (*Cancelled*)

2. (*Previously Presented*) The programmable circuit configurator of claim 6, wherein the dedicated test-signal circuitry includes a test-data input port adapted to pass test data to the dedicated test-signal circuitry, a test-data output port adapted to pass test data from the dedicated test-signal circuitry, and a test-clock port.

3. (*Cancelled*)

4. (*Previously Presented*) The programmable circuit configurator of claim 6, wherein the configured circuit includes a plurality of JTAG signal path switches adapted to route JTAG signals on the configured circuit and between the configured circuit and other configured circuits coupled to the configured circuit, and wherein the microcontroller is programmed to configure the plurality of JTAG signal path switches.

5. (*Previously Presented*) The programmable circuit configurator of claim 6, wherein the microcontroller is programmed to switch the plurality of JTAG signal path switches in response to the reconfiguration-control signals received at the user-controlled device and sent to the microcontroller via the communications link.

6. (*Previously Presented*) A programmable circuit configurator having an interface for coupling to a target circuit device and having dedicated test-signal circuitry for testing a configured circuit that includes the target circuit device, the programmable circuit configurator comprising:

routing circuitry on the configured circuit having configurable test signal routing paths with controllable switches therein for coupling test signals between the dedicated test-signal circuitry and the target circuit device via the interface;

a programmable microcontroller communicatively coupled to the routing circuitry, the microcontroller being programmed to control the controllable switches and thereby configure the test signal routing paths; and

a communications link adapted to communicatively couple an external user-controlled device and the programmable microcontroller for passing reconfiguration-control signals to the programmable microcontroller and for reporting characteristics of the configured test signal routing paths, the reconfiguration-control signals being communicatively coupled to the programmable microcontroller for reconfiguring the test signal routing paths, and

wherein the microcontroller is separably operable from the configured circuit and programmed to monitor operational characteristics of the configured circuit prior to power-up of the configured circuit.

7. (*Original*) The programmable circuit configurator of claim 6, wherein the microcontroller is programmed to monitor and configure the position of JTAG signal path switches on the configured circuit when the configured circuit is not powered.

8. (*Original*) The programmable circuit configurator of claim 7, wherein the microcontroller is programmed to set the position of the JTAG signal path switches when the configured circuit is not powered.

9. (*Previously Presented*) The programmable circuit configurator of claim 6, wherein control inputs from the user-controlled device are stored in memory at the programmable circuit configurator and wherein the microcontroller is programmed to configure the test signal path switches using the control inputs stored in the memory.

10. (*Previously Presented*) A programmable circuit configurator having an interface for coupling to a target circuit device and having dedicated test-signal circuitry for testing a configured circuit that includes the target circuit device, the programmable circuit configurator comprising:

routing circuitry on the configured circuit having configurable test signal routing paths with controllable switches therein for coupling test signals between the dedicated test-signal circuitry and the target circuit device via the interface;

a programmable microcontroller communicatively coupled to the routing circuitry, the microcontroller being programmed to control the controllable switches and thereby configure the test signal routing paths; and

a communications link adapted to communicatively couple an external user-controlled device and the programmable microcontroller for passing reconfiguration-control signals to the programmable microcontroller and for reporting characteristics of the configured test signal routing paths, the reconfiguration-control signals being communicatively coupled to the programmable microcontroller for reconfiguring the test signal routing paths, and

wherein the microcontroller is programmed to perform diagnostic testing on the configured circuit when the configured circuit is not powered.

11. (*Original*) The programmable circuit configurator of claim 10, wherein the microcontroller is programmed to send information obtained from the diagnostic testing to a user via the communications link and the user-controlled device.

12. (*Cancelled*)

13. (*Cancelled*)

14. (*Previously Presented*) A hardware configurator arrangement comprising:

a configured circuit having a plurality of controllable switches on the configured circuit communicatively coupled between at least two JTAG test nodes on JTAG signal paths and target circuit devices along the JTAG signal paths;

a programmable microcontroller communicatively coupled to the configured circuit, programmed to monitor and control a plurality of operational characteristics of the configured circuit including the controllable switches and adapted to output data in response to the monitored operational characteristics;

a user interface adapted to accept control inputs from a user and to provide the output data from the microcontroller to the user;

a communications link configured and arranged to communicate the control inputs and the microcontroller output data between the microcontroller and the user interface;

and the microcontroller being programmable by the control inputs received from the user interface and communicated via the communications link for monitoring and controlling the plurality of operational characteristics of the programmable microcontroller, including controlling the controllable switches for coupling test signals to the target circuit devices;

wherein the microcontroller is programmed to automatically detect a test signal at one of the JTAG test nodes and, in response to an automatically detected test signal, to control the controllable switches to route data between at least one of the JTAG test nodes and at least one of the JTAG signal paths; and

wherein the microcontroller is programmed to monitor the JTAG test nodes using an interrupt routine for automatically detecting test signals at the JTAG test nodes.

15. (*Previously Presented*) The hardware configurator arrangement of claim14, wherein the microcontroller is programmed to control the controllable switches for routing JTAG test data between the configured circuit and another configured circuit.

16. (*Original*) The hardware configurator arrangement of claim 15, wherein said configured circuit is coupled to said other configured circuit such that physical access to the controllable switches is prevented.

17. (*Previously Presented*) The hardware configurator arrangement of claim 14, wherein the microcontroller is adapted to control operation of the configured circuit in response to control inputs from the user interface.

18. (*Previously Presented*) The hardware configurator arrangement of claim 14, wherein the microcontroller is adapted to control JTAG operation of the configured circuit in response to control inputs from the user interface.

19. (*Cancelled*)

20. (*Cancelled*)

21. (*Previously Presented*) The configurator server of claim 22 wherein the microcontroller is adapted to set the JTAG test signal routing switches in response to the control inputs received from the user interface.

22. (*Previously Presented*) For use in a prototype arrangement of inter-connectable circuit boards, each of the inter-connectable circuit boards having JTAG test signal routing switches, JTAG test nodes and at least two JTAG circuit paths, a configurator server comprising:

a memory adapted to store data including program software;

a reprogrammable microcontroller on a first one of the inter-connectable circuit boards and communicatively coupled to the memory, the microcontroller being programmed to automatically configure the JTAG test signal routing switches in response to a signal detected from at least one of the JTAG test nodes for routing JTAG test signals along a JTAG circuit path on at least the first one of the inter-connectable circuit boards using data stored in the memory including the program software;

wherein the microcontroller is programmed to perform an interrupt routine for detecting the signal from the at least one of the plurality of test nodes;

and a communications link adapted to communicate control inputs from a user interface device to the microcontroller and to communicate outputs from the microcontroller to the user interface, the microcontroller being operable in response to the control inputs;

23. (*Previously Presented*) The configurator server of claim 22, wherein each of the inter-connectable circuit boards includes at least one JTAG input test node and at least one JTAG output test node and wherein the JTAG output test node of the first one of the inter-connectable circuit boards is coupled to a JTAG input test node of a second one of the inter-connectable circuit boards and wherein the microcontroller is programmed for automatically configuring the JTAG test signal routing switches to route JTAG test signals between the first and second inter-connectable circuit boards via the JTAG output and JTAG input test nodes.

24. (*Cancelled*)

25. (*Cancelled*)